ABSTRACT OF THE DISCLOSURE

A digital signal processor. The digital signal processor includes a content addressable memory (CAM) array for storing entries. The digital signal processor includes a partitioned priority index table having a plurality of rows and columns of priority blocks. Each row of the plurality of rows of priority blocks is capable of storing a priority number associated with an entry in the CAM array. Each column of the plurality of columns of priority blocks has compare logic coupled to each of the priority blocks in its respective column. The digital signal processor includes an encoder coupled to the partitioned priority index table.